

09/966124
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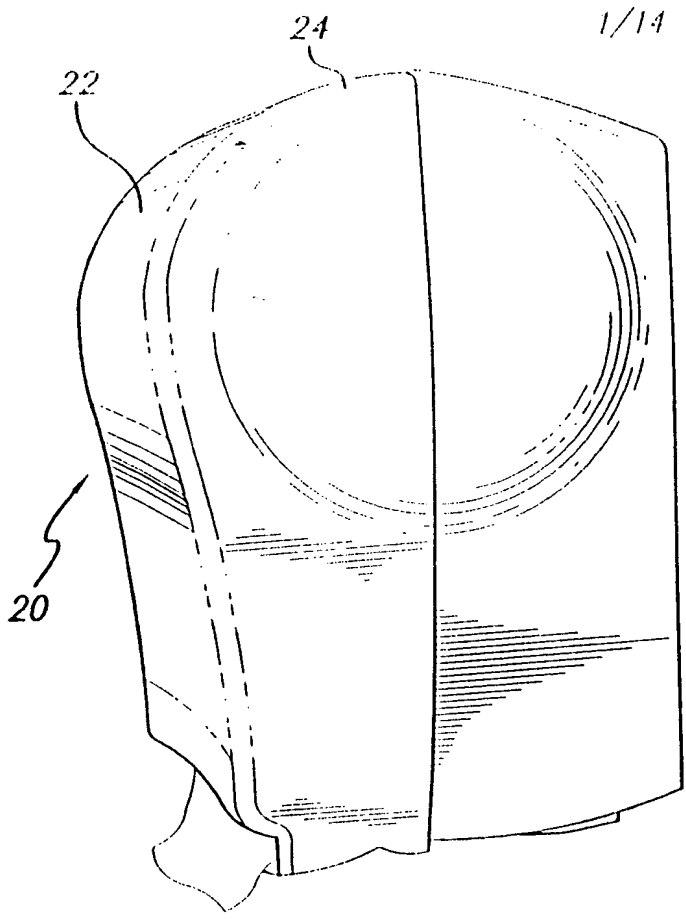


FIG. 1

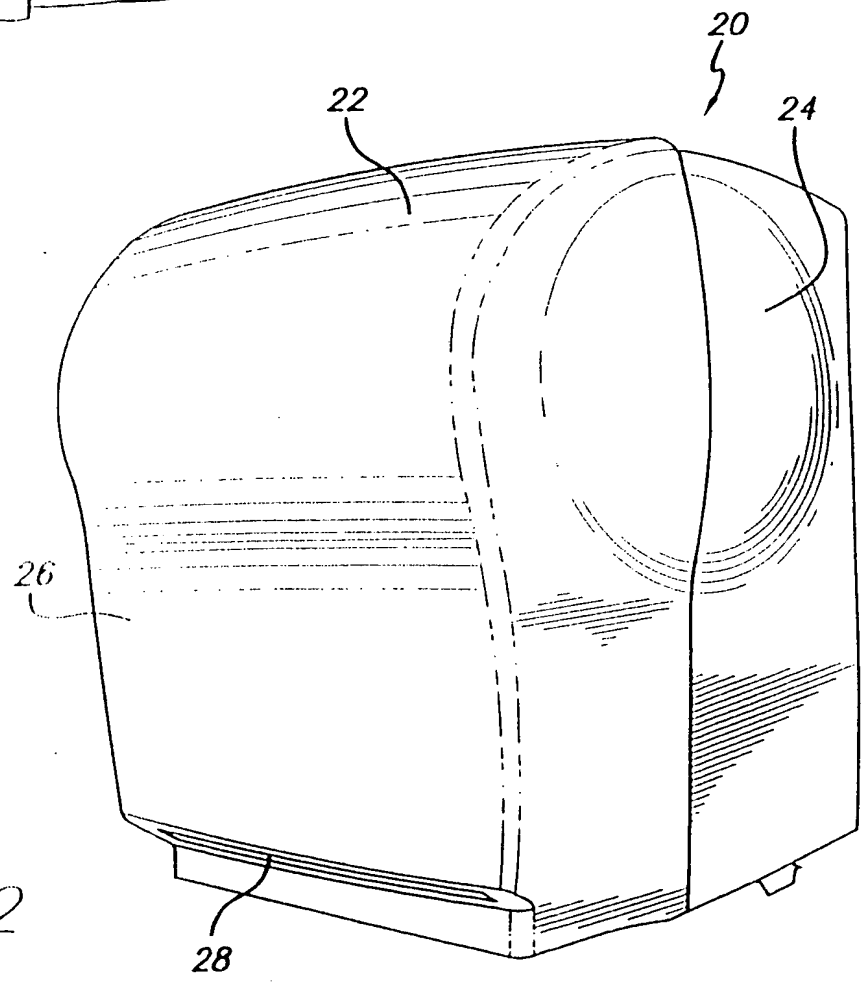


FIG. 2

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FIG. 3

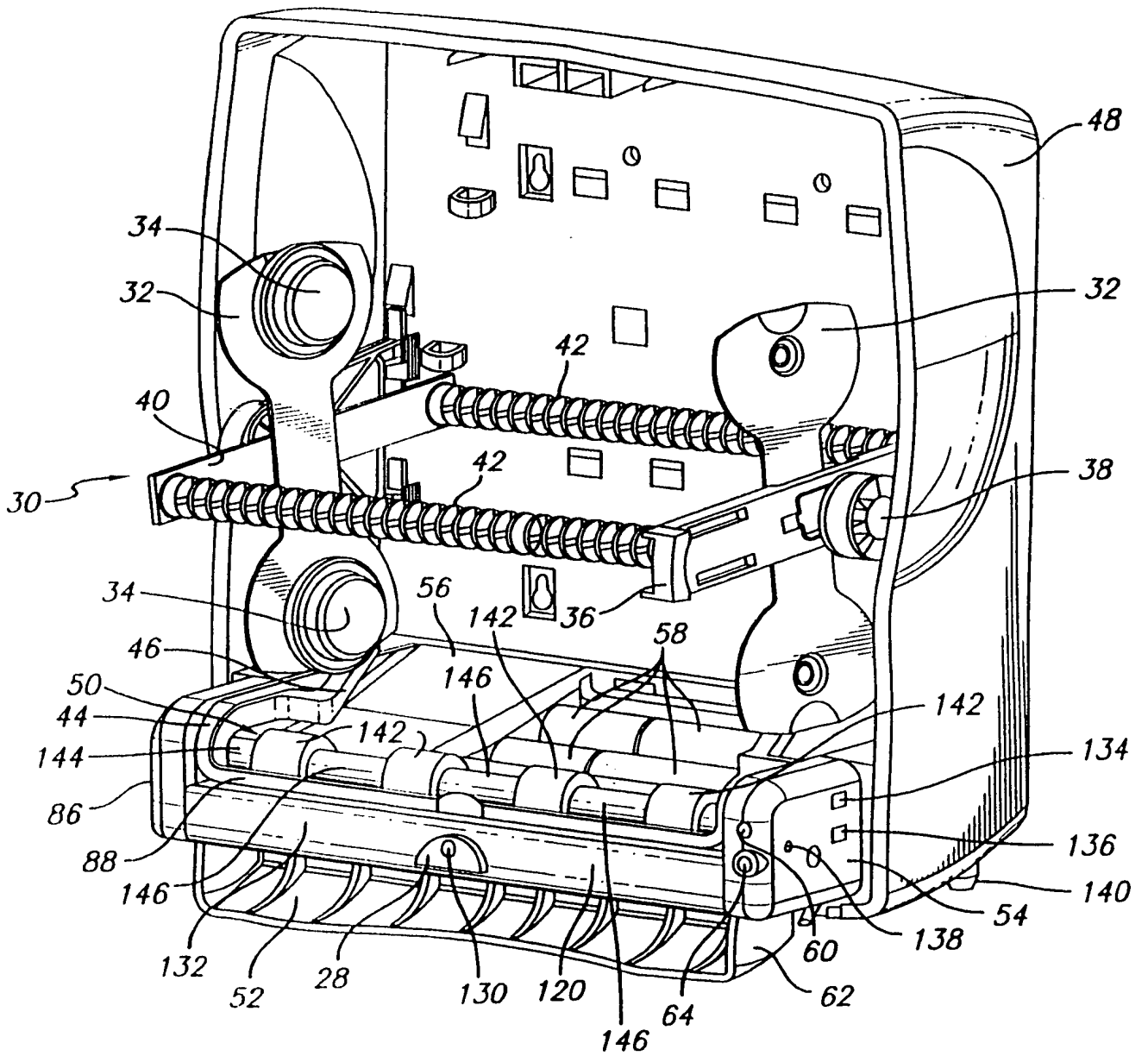
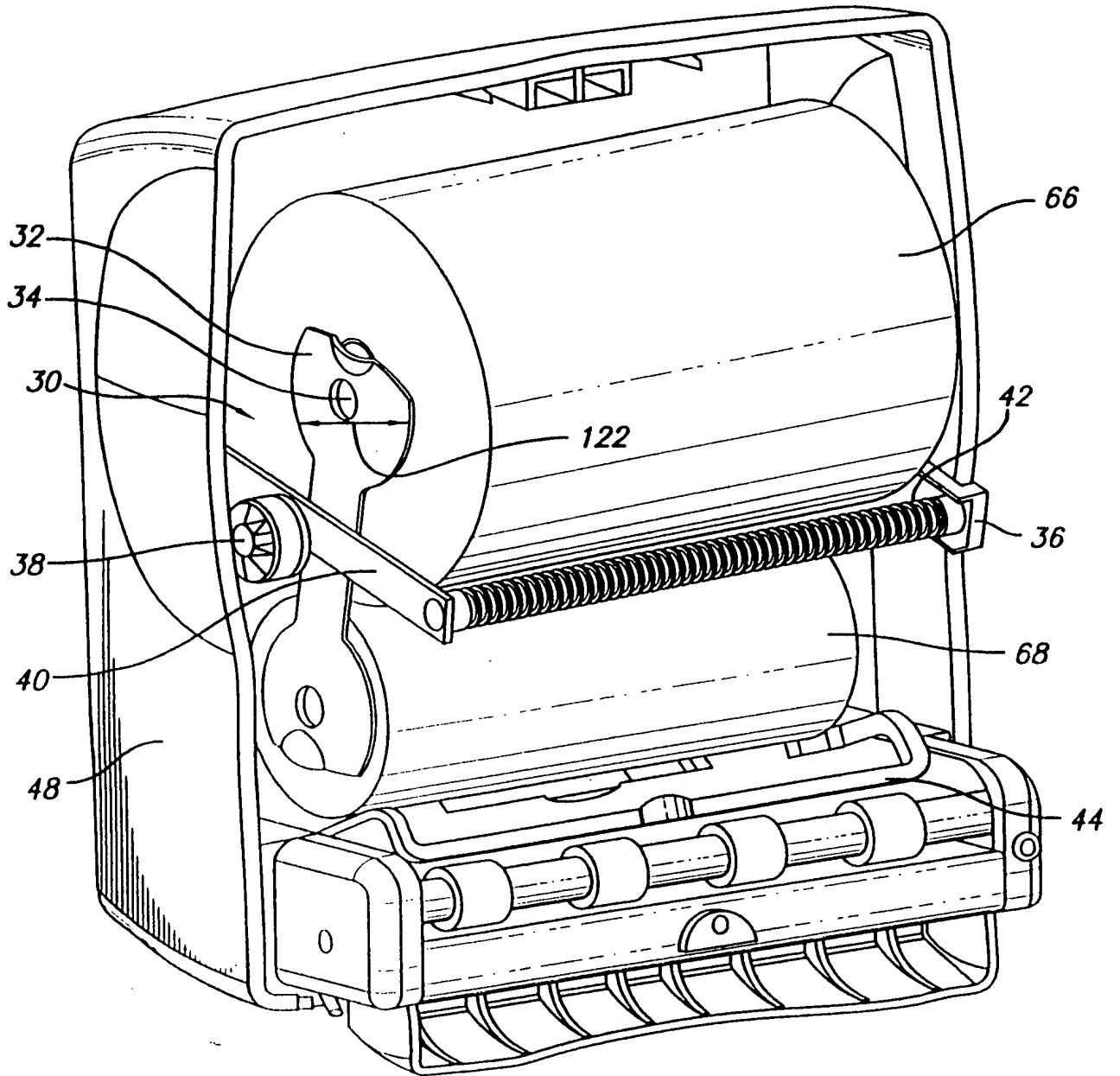


FIG. 4A



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FIG. 4B

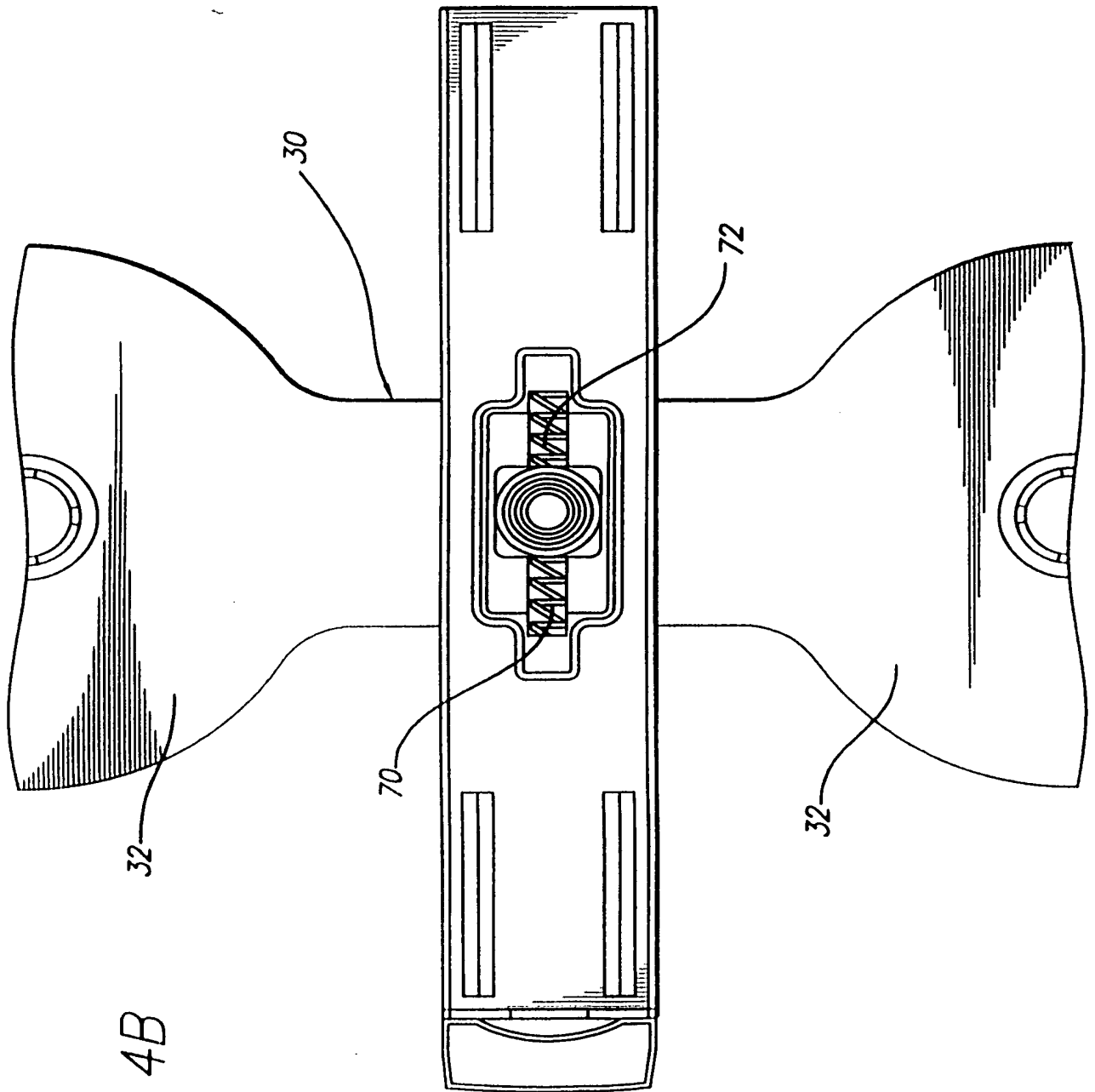


FIG. 4C

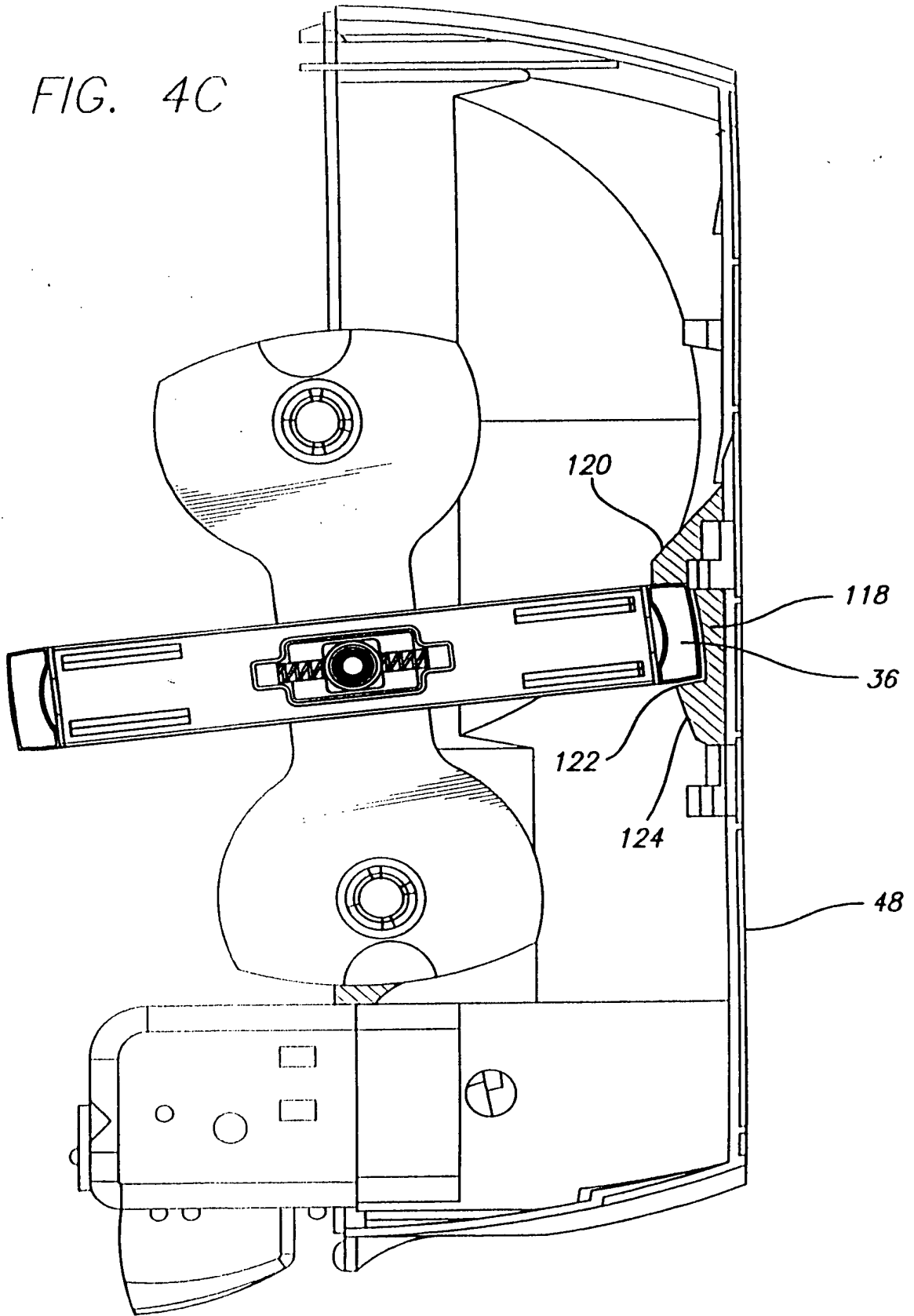


FIG. 5

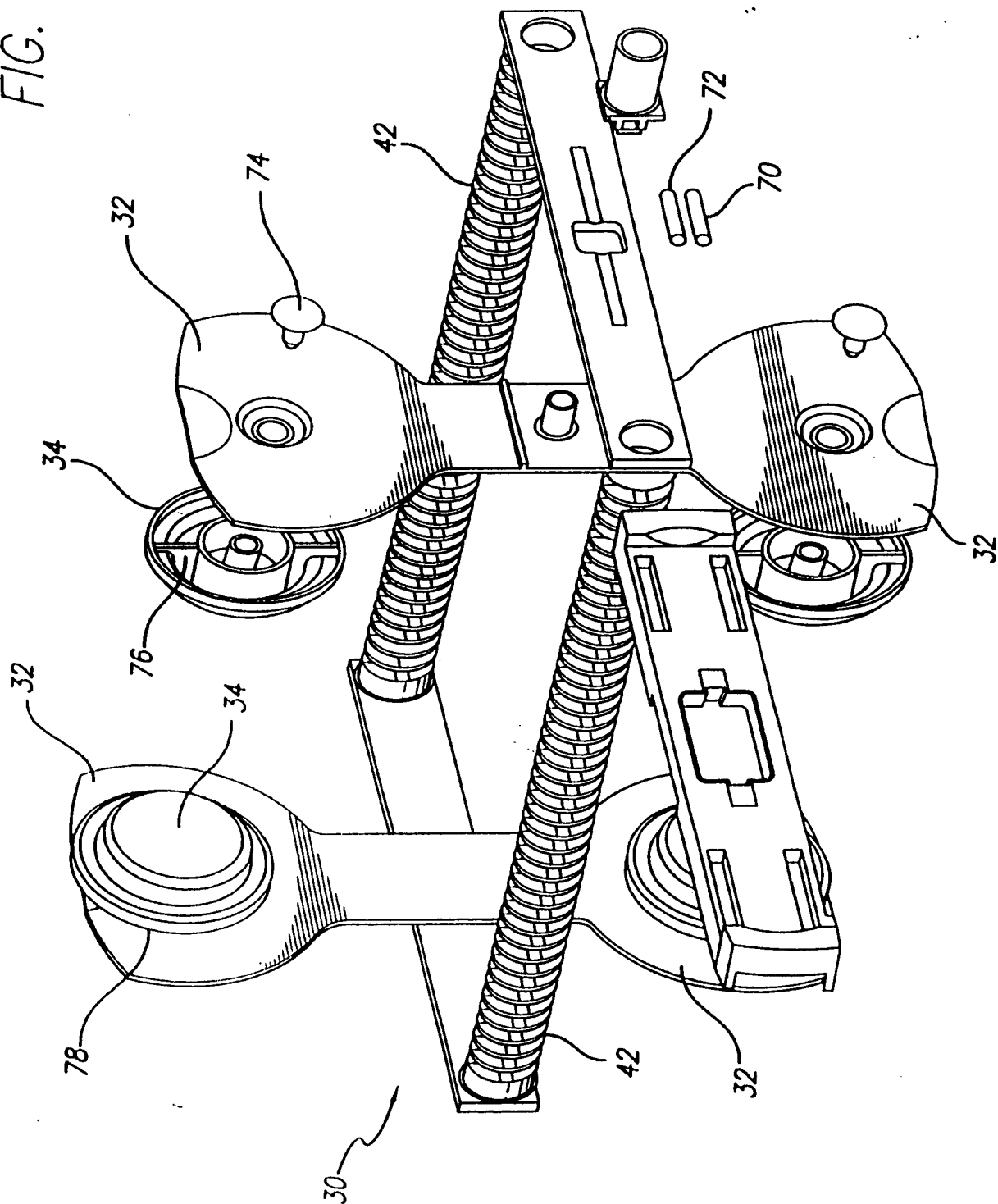


FIG. 6A

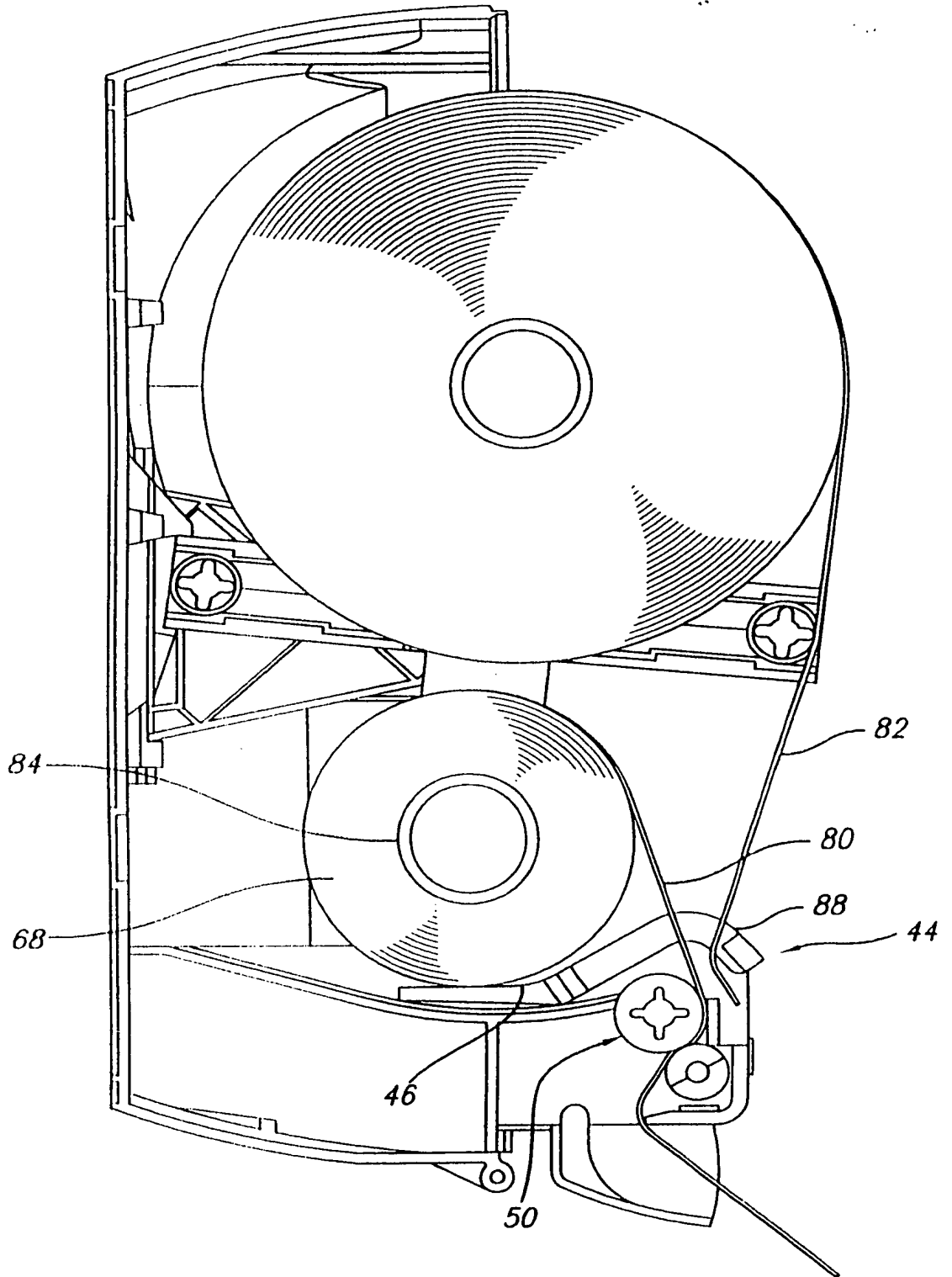
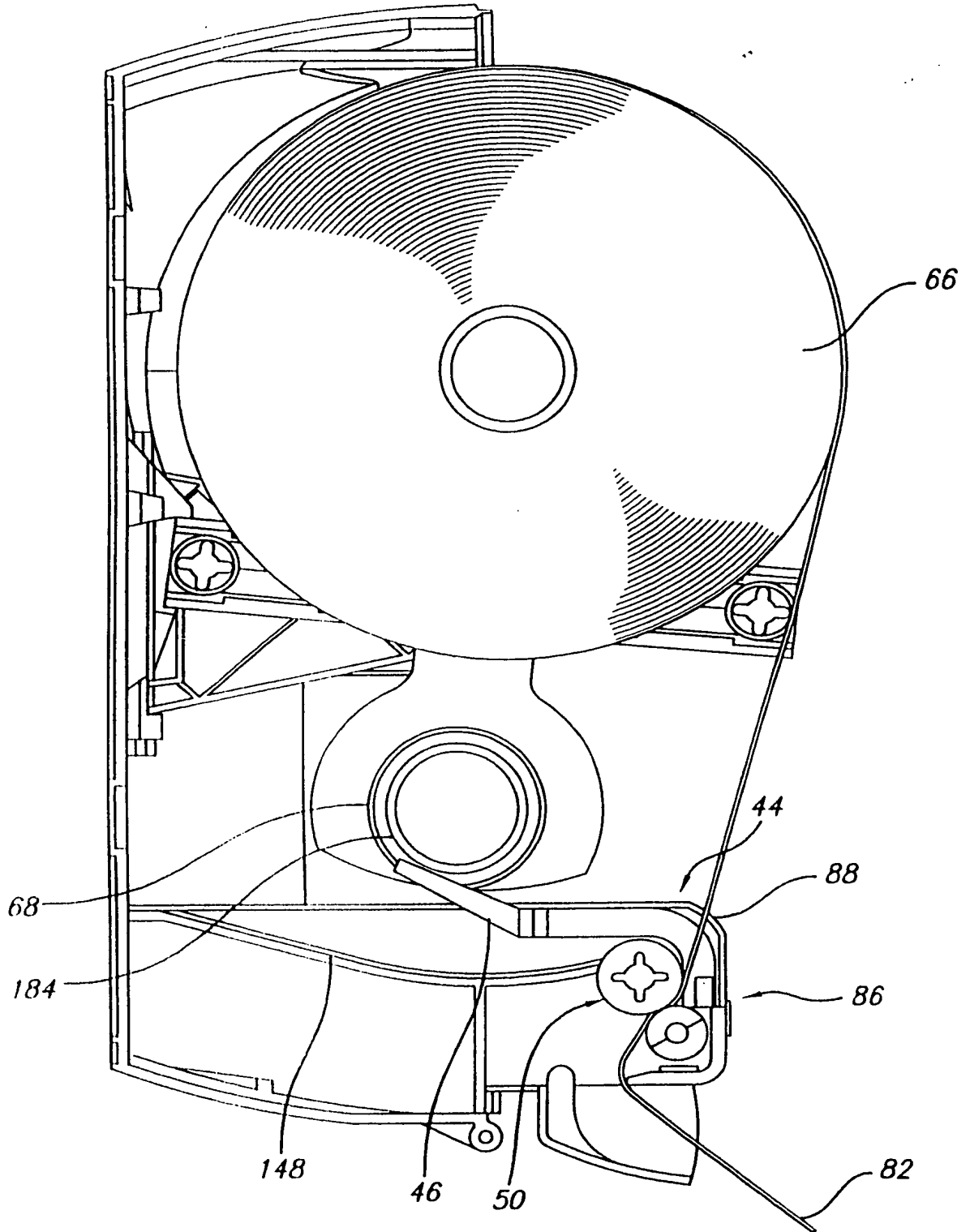


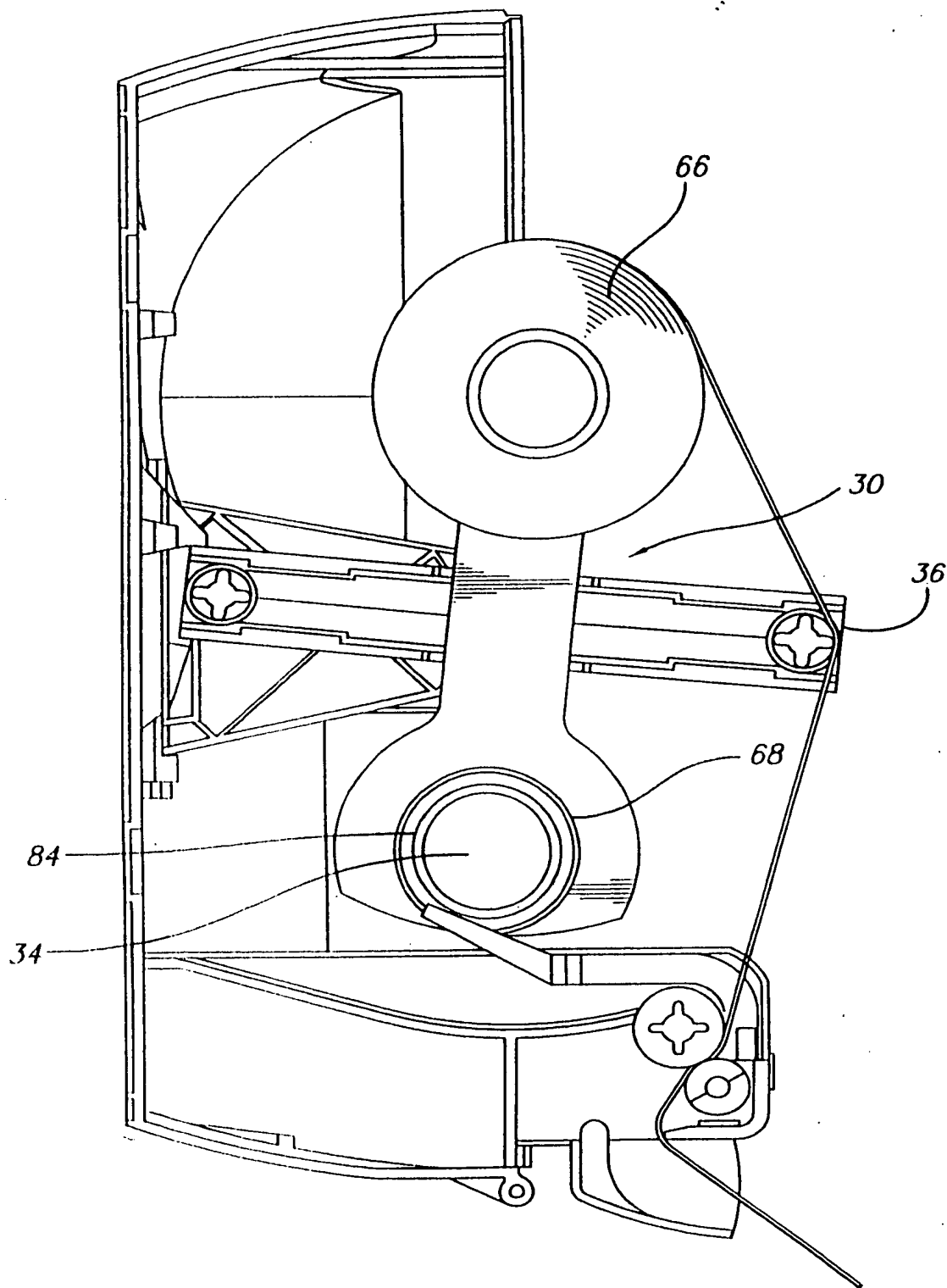
FIG. 6B



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FIG. 7A



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FIG. 7B

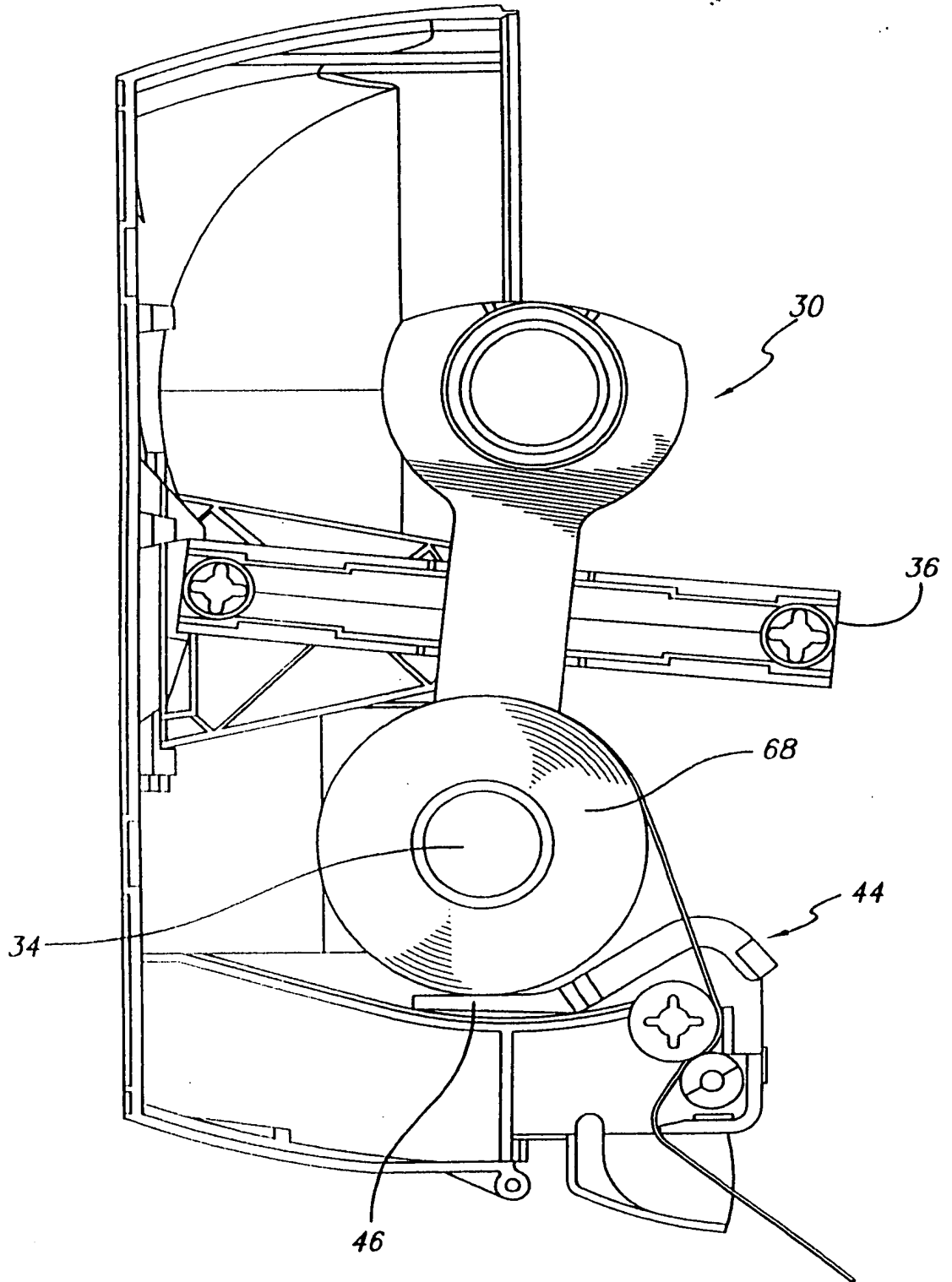


FIG. 7C

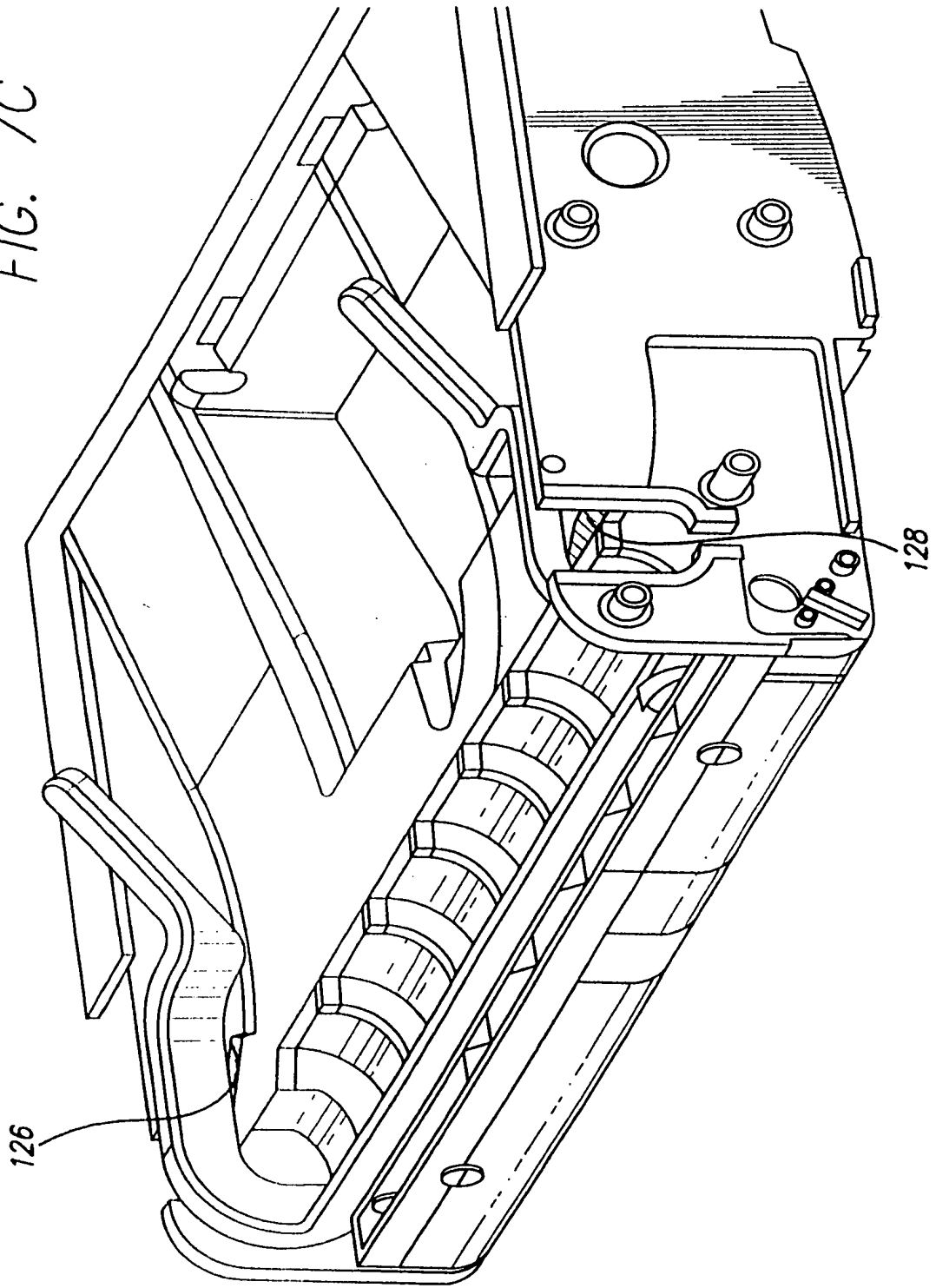


FIG. 7D

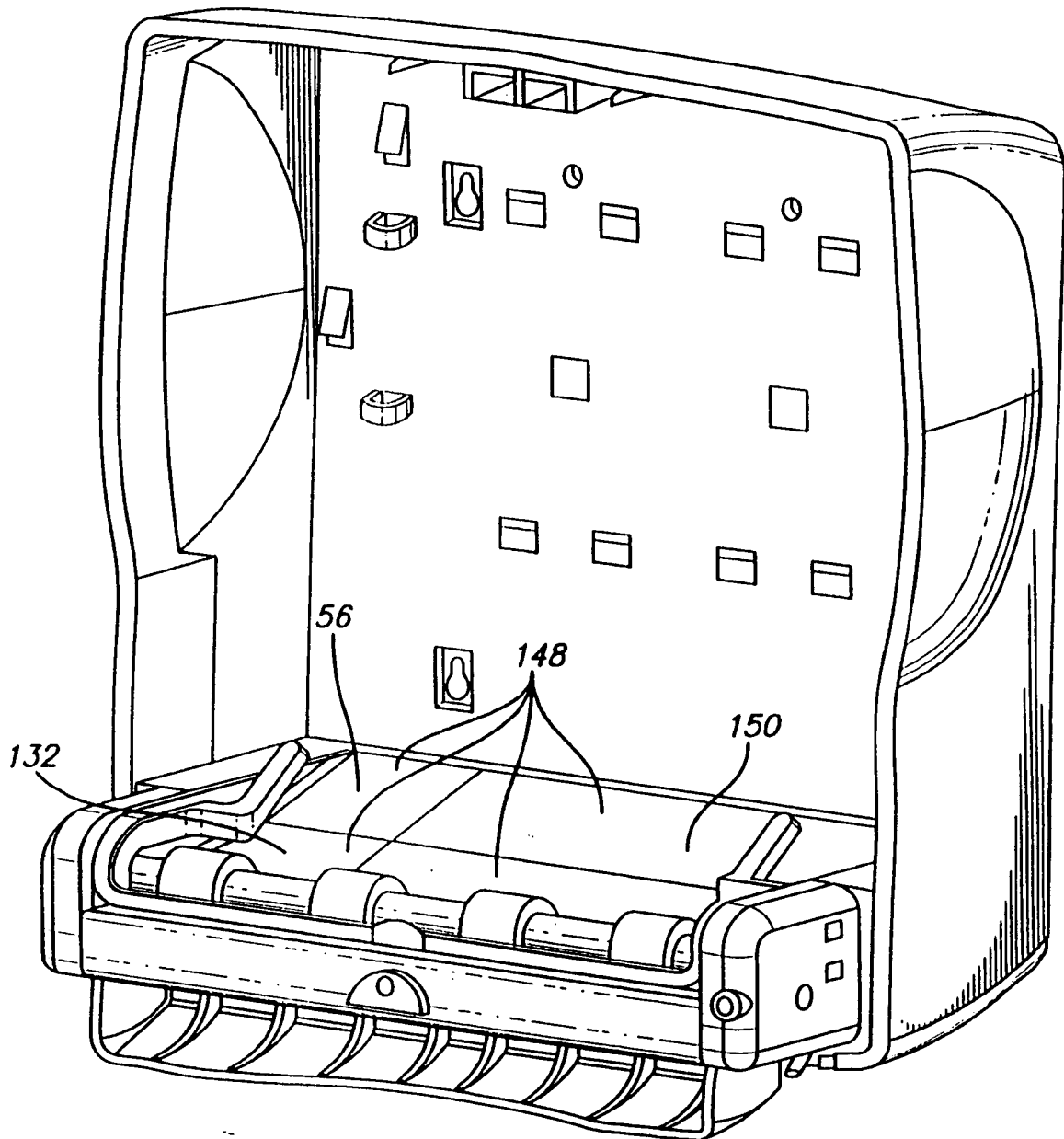
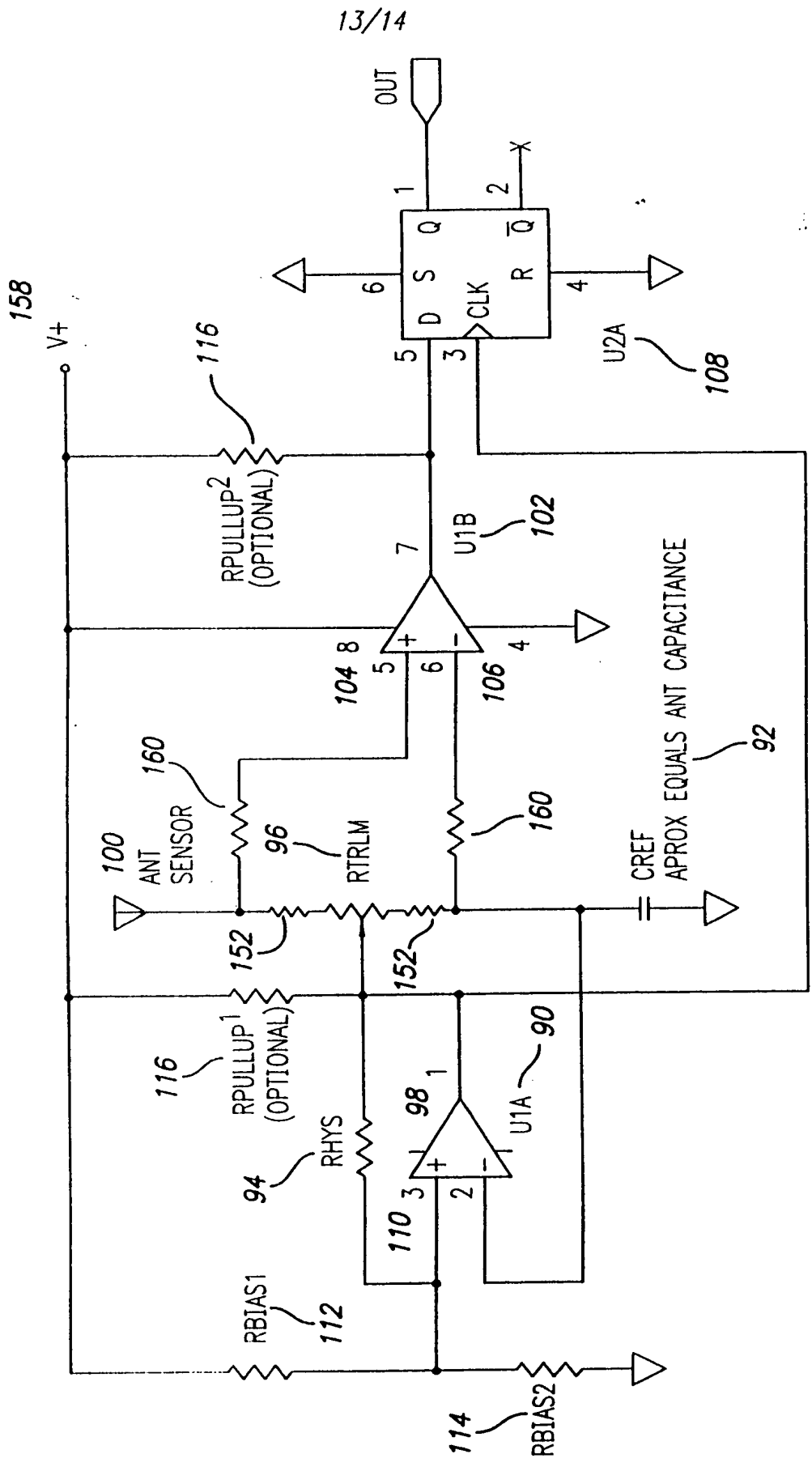


FIG. 8A



The diagram shows a multi-stage amplifier circuit. It begins with a differential input stage consisting of transistors Q1, Q2, Q3, and Q4. The inputs are labeled '+INPUT' and '-INPUT'. The circuit is biased by a current source V1, which is connected to the bases of Q2 and Q3 through four $1.1\mu A$ current sources. The output of this stage is connected to the base of transistor Q7. Transistor Q7 is part of a second stage that drives the input of an LM 393 open collector comparator, labeled 154. The output of the LM 393 is connected to the input of a TLC 3702 CMOS push-pull output stage, labeled 158. The TLC 3702 stage has two outputs, both labeled 156, which are connected to a load VI. The output of the LM 393 is also labeled 'OUTPUT'.

The timing diagram shows three waveforms over time. The top waveform, labeled 'CLOCK, U1A, pin1', is a square wave. The middle waveform, labeled 'ANT, U1B, pin5', is a sawtooth wave. The bottom waveform, labeled 'CREF, U1B, pin6', is also a sawtooth wave. Arrows on the right side of the diagram point to each waveform, labeled A, B, and C respectively.

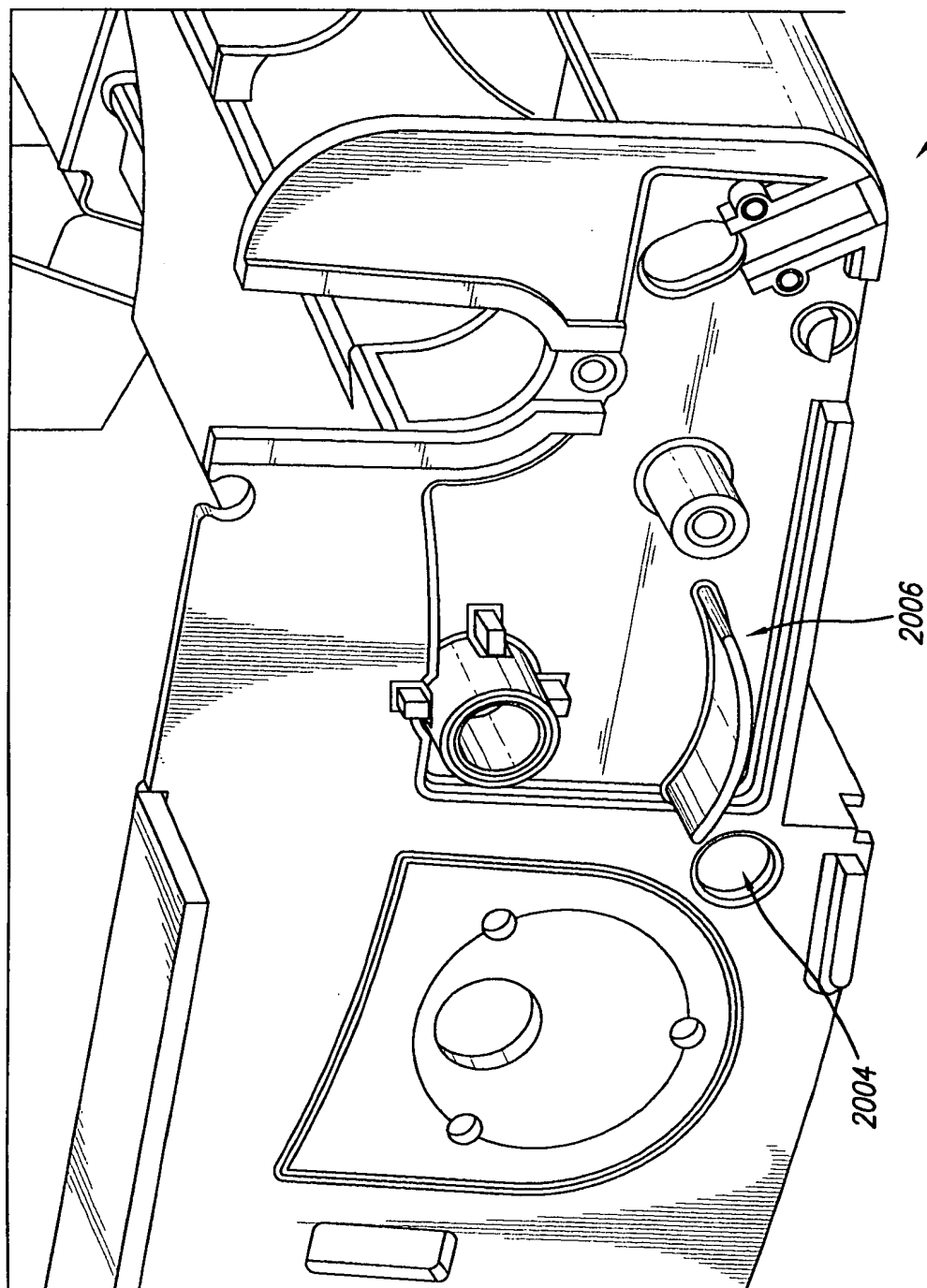


FIG. 10A

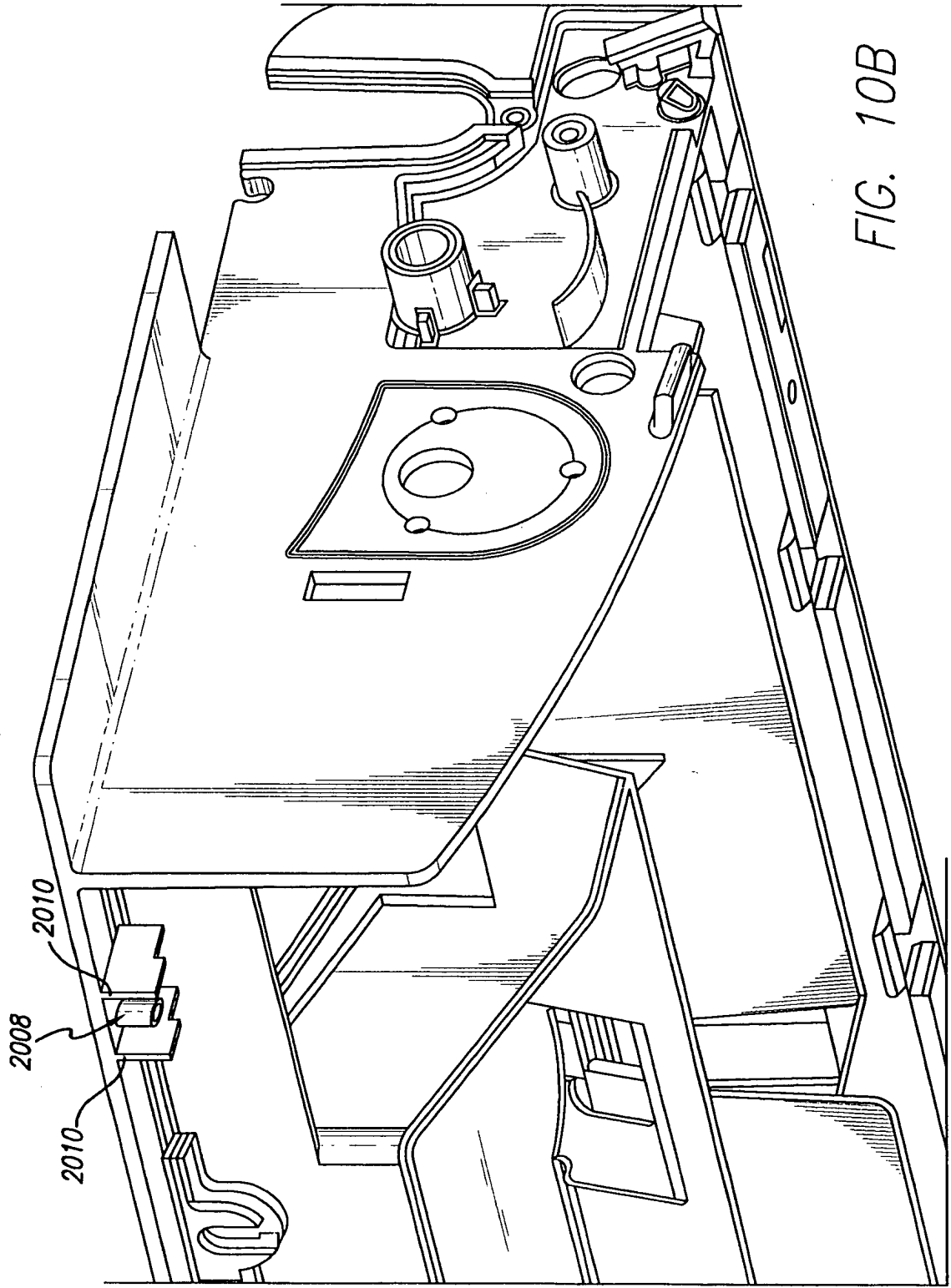


FIG. 10C

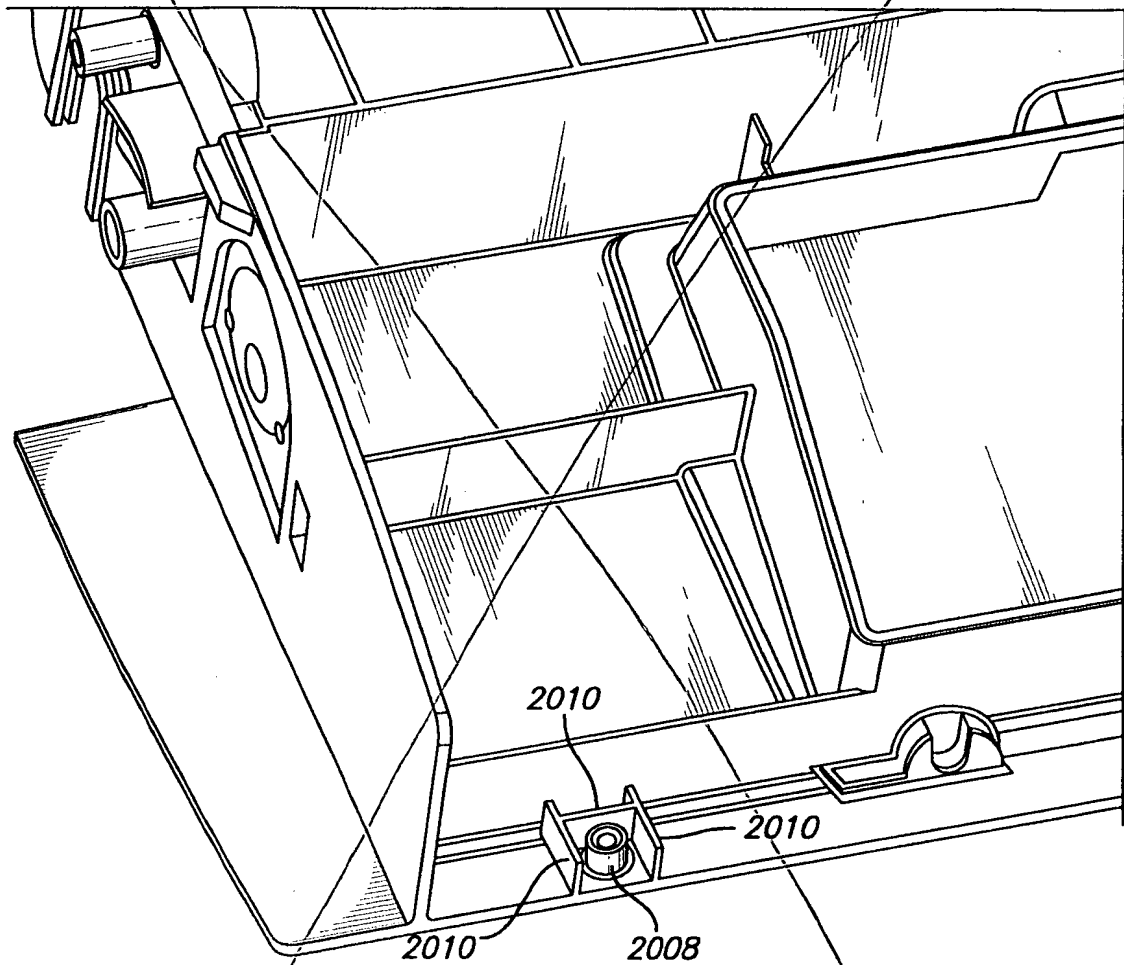
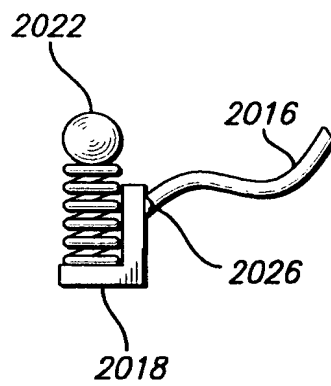


FIG. 15



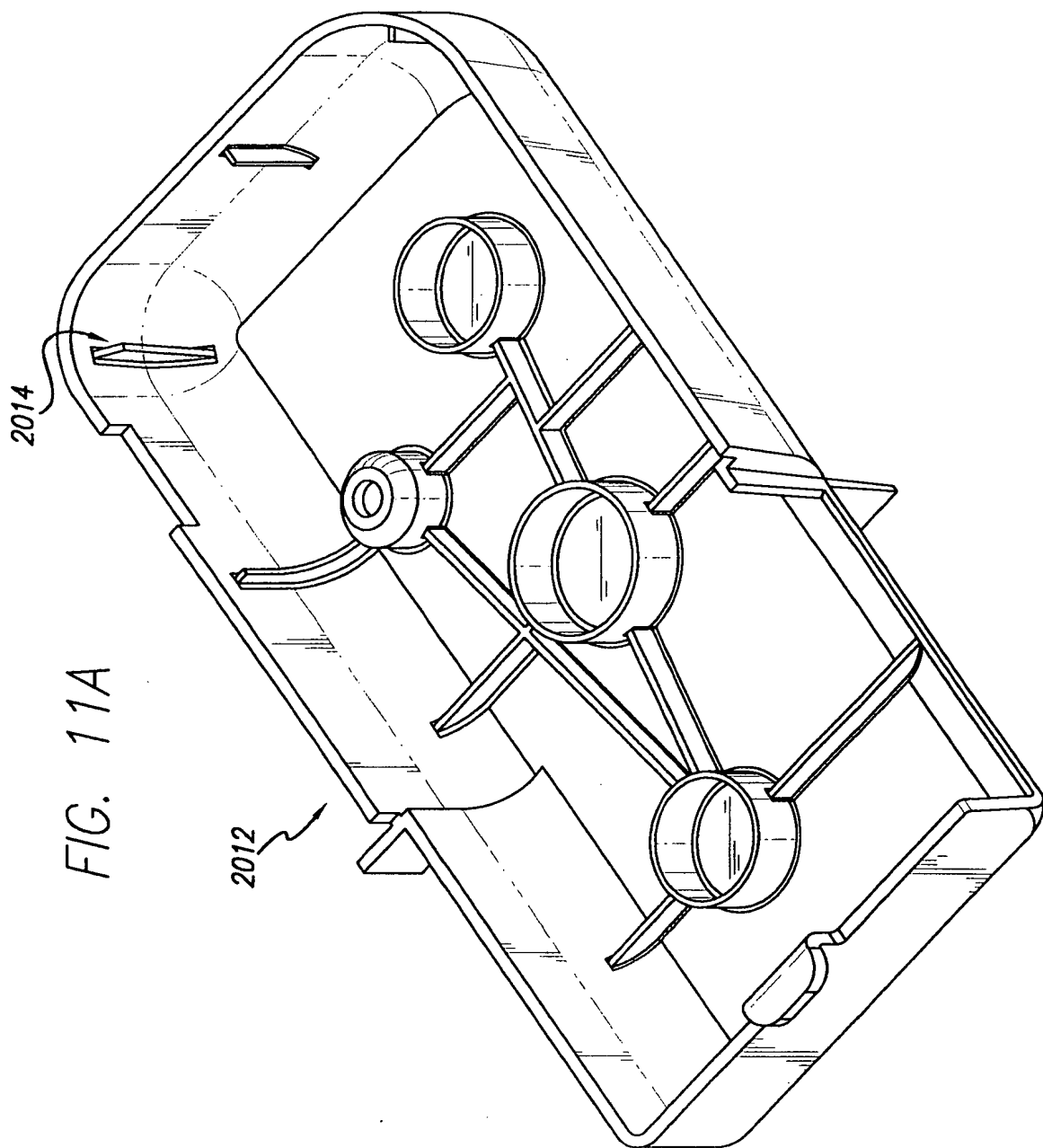


FIG. 11B

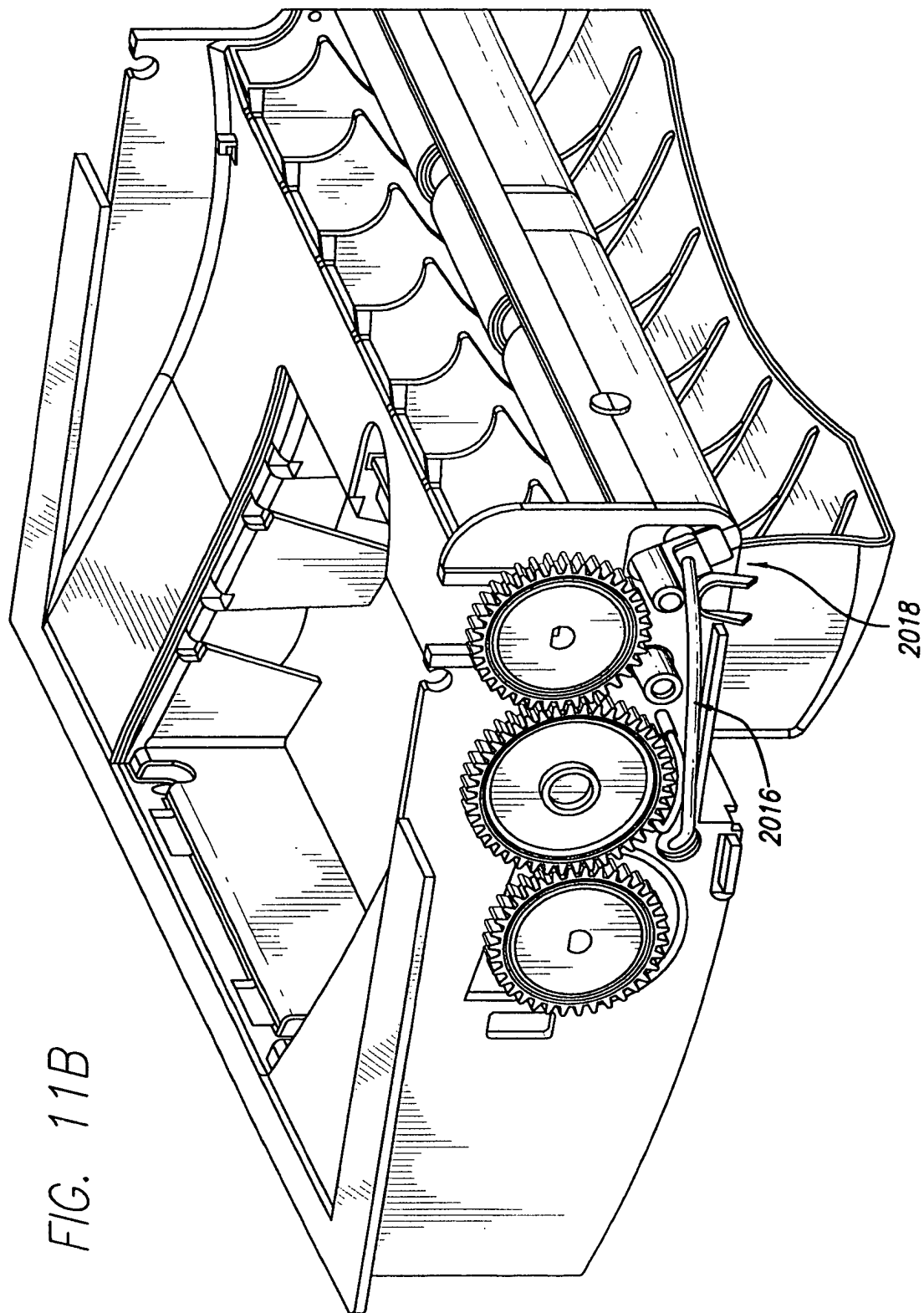


FIG. 11C

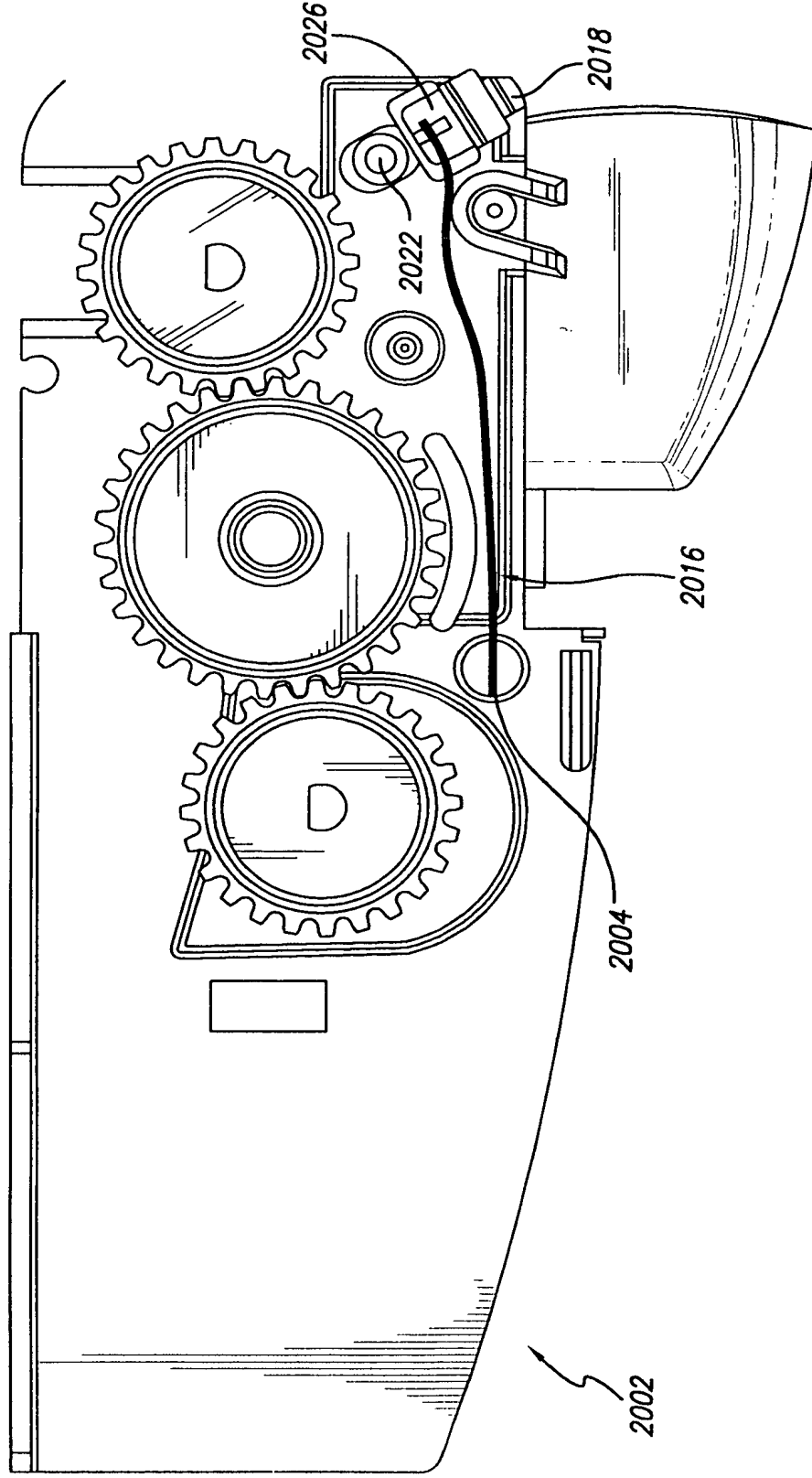


FIG. 12

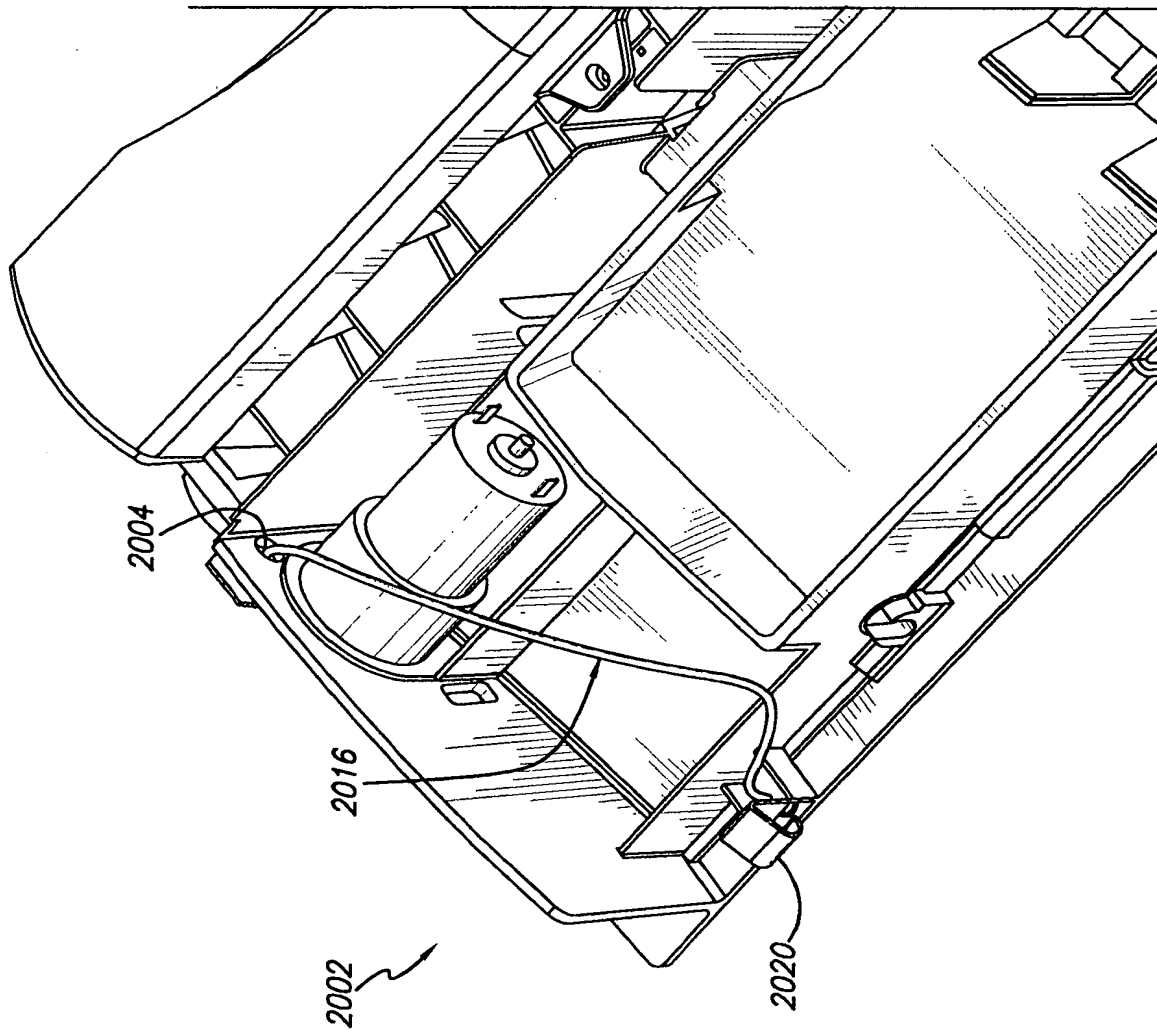


FIG. 13A

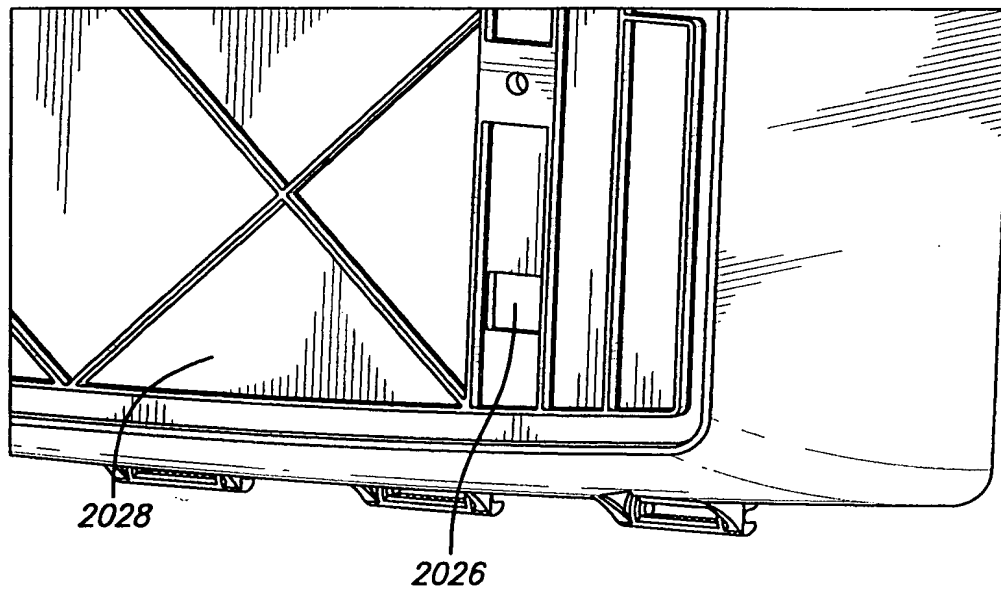


FIG. 13B

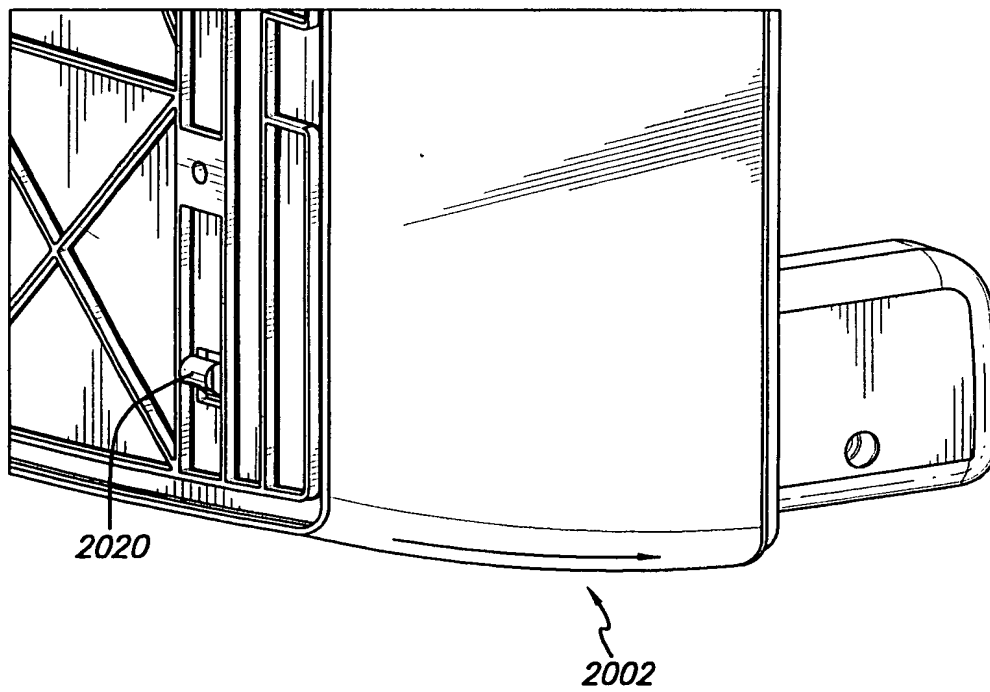


FIG. 14

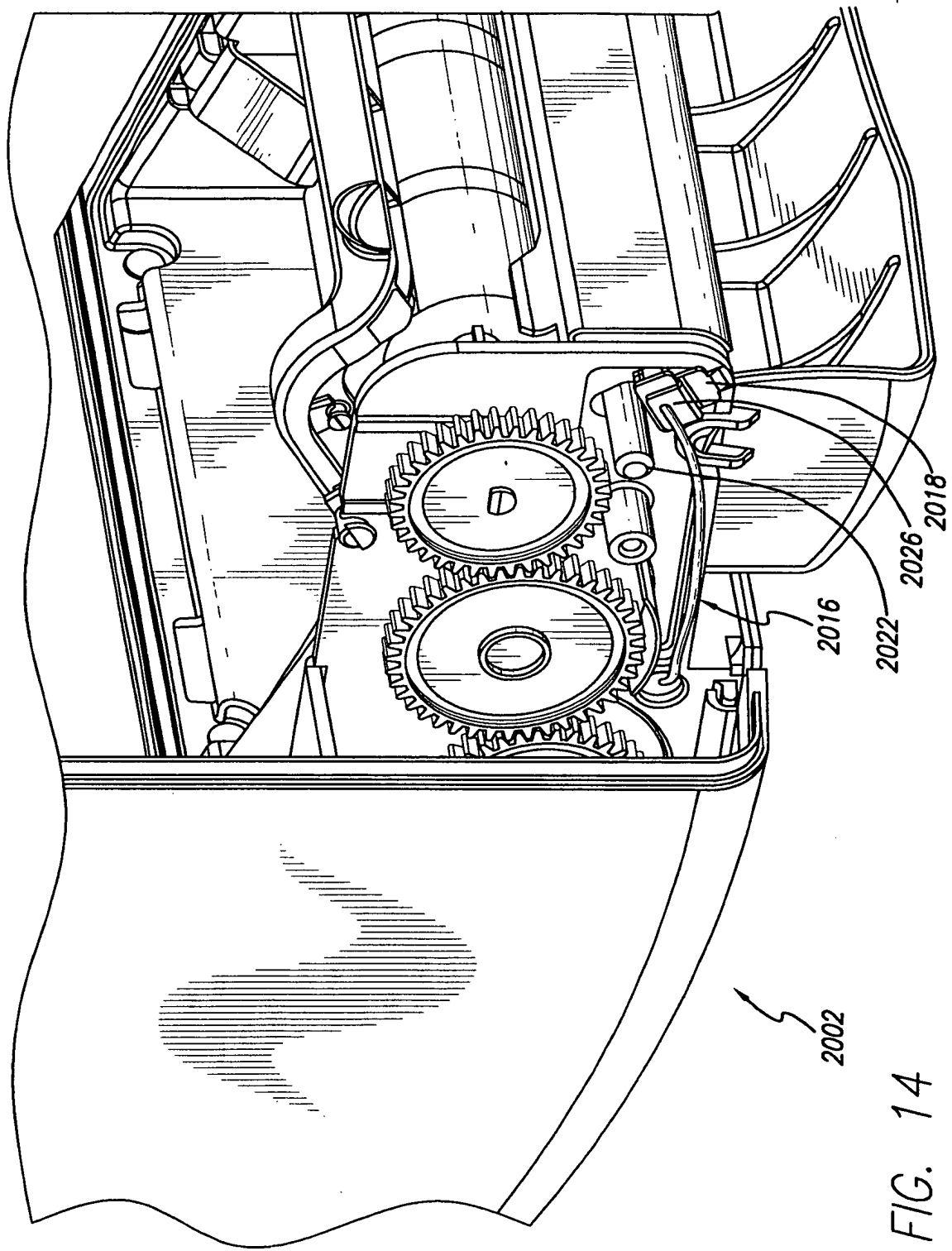


FIG. 14